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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,105	12/15/2001	Roberto Coccioli	01CON281P	5802

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n No.	Applicant(s)	
	10/020,105	COCCIOLI ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 8, 9, 11-14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al. (US Pat. 5786738) in view of Sholley et al. (US Pat. 6265774).

Regarding claim 1, Ikata et al. disclose a structure comprising:

- a ceramic laminate substrate (CLS- 62 in Fig. 14) having a plurality of layers (62_1-62_4) having a ground and signal patterns (Col. 8, line 60- Col. 9, line 8) and a top surface (63 in Fig. 14) for receiving a semiconductor die (64 in Fig. 14)
- an antenna element (68 in Fig. 14) situated on a bottom surface of the substrate (67 in Fig. 14 and 11), the antenna element comprising the antenna pattern/circuit pattern having a meandering line pattern (68 in Fig. 14; Col. 9, line 20) suitable for connection to the die

- a laminate substrate reference pad/pattern in the CLS (72 in Fig. 14), the reference pad/pattern being a grounding pad/pattern situated over the antenna element, and
- signal and ground antenna terminals/pads (66a-d in Fig. 14 and 66d) being situated at a side/periphery of the antenna element on the bottom surface of the CLS, the antenna terminals/pads to be electrically connected to another circuit board/printed circuit board/PCB (Col. 8, line 60)

(Fig. 14 and 15; Col. 10, line 16-46; Col. 8-10).

Ikata et al. fail to teach:

a) at least one laminate substrate reference via being situated at a side of the antenna, and

b) the antenna pattern/element being the antenna.

a) Ikata et al. further teach in another embodiment of Fig. 2B, the CLS having a plurality of substrate layers (32_1-32_4 in Fig. 2B), the layers having predetermined ground and signal patterns where a plurality of through holes/vias (through holes/vias not being numerically referenced in Fig. 2A and B; Col. 5, line 1-36) in the substrate layers link/electrically connect the respective reference/ground and signal patterns/terminals (36a, 36b, etc. in Fig. 2B) situated at a side of the antenna element and the bottom surface of the substrate.

b) Sholley et al. teach a conventional high frequency/RF packages where interconnection patterns and leads/terminals connecting a RF component serve/act as an antenna itself operating at full wave or half-wave picking up transmission or radiating energy as required by the circuit applications (Col. 1, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate at least one laminate substrate reference via being situated at a side of the antenna element as taught by the embodiment of Fig. 2B in Ikata et al. and the antenna element/pattern being the antenna as taught by Sholley et al. so that the signal leakage can be reduced and the transmission signal propagation and the shielding effect can be improved in Ikata et al's structure.

Regarding claim 2, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Ikata et al. teach the laminate substrate reference pad (72 in Fig. 14) being the ground pad.

Regarding claim 3, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Ikata et al. teach the laminate substrate reference via (through holes/vias not being numerically referenced in Fig. 2A and B; Col. 5, line 1-36) being the ground via.

Regarding claim 4, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Ikata et al. teach the laminate substrate reference via being electrically connected to the respective reference pad (through holes/vias not being numerically referenced in Fig. 2A and B; Col. 5, line 1-36).

Regarding claim 8, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Ikata et al. teach the laminate substrate (62 in Fig. 14; Col. 9, line 10) being ceramic.

Regarding claim 9, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Ikata et al. the antenna comprises the meandering line pattern (68 in Fig. 14; Col. 9, line 20).

Regarding claim 11, Ikata et al. disclose a structure comprising:

- a ceramic laminate substrate (CLS- 62 in Fig. 14) having a plurality of layers (62_1-62_4) having a ground and signal patterns (Col. 8, line 60- Col. 9, line 8) and a top surface (63 in Fig. 14) for receiving a semiconductor die (64 in Fig. 14)
- an antenna element (68 in Fig. 14) situated on a bottom surface of the substrate (67 in Fig. 14 and 11), the antenna element comprising the antenna pattern/circuit pattern an meandering line pattern (68 in Fig. 14; Col. 9, line 20) suitable for connection to the die

- a laminate substrate reference pad/pattern in the CLS (72 in Fig. 14), the reference pad/pattern being a grounding pad/pattern situated over the antenna element, and
- signal and ground antenna terminals/pads (66a-d in Fig. 14 and 66d) being situated at a side/periphery of the antenna element on the bottom surface of the CLS, the terminals/pads to be electrically connected to another circuit board/printed circuit board/PCB (Col. 8, line 60)

(Fig. 14 and 15; Col. 10, line 16-46; Col. 8-10).

Ikata et al fail to teach:

a) the antenna pattern/element being the antenna, and

b) a plurality of laminate substrate reference vias, each of them being situated at a side of the antenna

a) Ikata et al. further teach in the embodiment of Fig. 2B, the CLS having a plurality of substrate layers (32_1-32_4 in Fig. 2B), the layers having predetermined ground and signal patterns where a plurality of through holes/vias (through holes/vias not being numerically referenced in Fig. 2A and B; Col. 5, line 1-36;) in the substrate layers link/electrically connect the respective reference/ground and signal patterns/terminals (36a, 36b, etc. in Fig. 2B) situated at a side of the antenna element and the bottom surface of the substrate.

b) Sholley et al. teach the conventional high frequency/RF packages where interconnection patterns and leads/terminals connecting a RF component serve/act as an antenna itself operating at full wave or half-wave picking up transmission or radiating energy as required by the circuit applications (Col. 1, lines 45-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate each of the plurality of laminate substrate reference vias being situated at a side of the antenna element as taught in the embodiment of Fig. 2A/2B in Ikata et al. and the antenna element/pattern being the antenna as taught by Sholley et al. so that the signal leakage can be reduced and the transmission signal propagation and the shielding effect can be improved in Ikata et al's structure.

Regarding claim 12, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 11 above, wherein Ikata et al. teach the laminate substrate reference pad (72 in Fig. 14) being the ground pad.

Regarding claim 13, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 11 above, wherein Ikata et al. teach the laminate substrate reference via (through holes/vias not being numerically referenced in Fig. 2A and B; Col. 5, line 1-36) being the ground via.

Regarding claim 14, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 11 above, wherein Ikata et al. teach the laminate substrate reference via being electrically connected to the respective reference pad (through holes/vias not being numerically referenced in Fig. 2A and B; Col. 5, line 1-36).

Regarding claim 18, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 11 above, wherein Ikata et al. teach the laminate substrate (62 in Fig. 14; Col. 9, line 10) being ceramic.

Regarding claim 19, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 11 above, wherein Ikata et al. teach the antenna comprises the meandering line pattern (68 in Fig. 14; Col. 9, line 20).

3. Claims 5-7, 10, 15-17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikata et al. (US Pat. 5786738) and Sholley et al. (US Pat. 6265774) as applied to claims 1 and 11 above, and further in view of Houghton et al. (US Pat. 6282095 B1).

Regarding claims 5 and 6, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, except at least one laminate substrate reference via being electrically connected to the PCB reference via and the PCB via being connected to respective pad respectively.

Houghton et al. teach using a high frequency package comprising an antenna/heat sink element, the package including:

- a substrate comprising a dielectric material including a ceramic or a plastic/organic (Col. 2, line 22)
- connecting pads/terminals (40, 42, etc. in Fig. 1) comprising a variety of configurations such as pins, solder balls, etc. (Col. 5, line 10-25), and
- the package being connected to a PCB (10 in Fig. 1) where the pads/terminals of the package and the board (40/28 respectively in Fig. 1) are electrically connected to respective reference/ground vias (40/28and 26 respectively in Fig. 1) in the PCB to provide improved shielding around the device and the desired noise reduction (Col. 2, line 60- Col. 3, line 60)

(Fig. 1; Col. 4, line 65- Col. 5, line 10).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate at least one at least one laminate substrate reference via being electrically connected to the PCB reference via and PCB via being connected to respective pad as taught by Houghton et al. so that the shielding effect can be improved and high frequency noise can be reduced in Sholley et al. and Ikata et al's structure.

Regarding claim 7, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claims 1 above, except the laminate substrate comprising an organic material.

Houghton et al. further teach the laminate substrate comprising an organic material (Col. 2, line 22).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the laminate substrate comprising an organic material as taught by Houghton et al. so that the mismatch in the thermal properties between the substrate and the PCB can be reduced and the processing can be simplified in Sholley et al. and Ikata et al's structure.

Regarding claim 10, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 1 above, except the laminate substrate reference via being electrically connected to the ball pad on the bottom surface of the laminate substrate.

Houghton et al. further teach using the substrate pads/terminals comprising balls, pins, leads, etc (Col. 5, line 10-25).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the laminate substrate reference via being electrically connected to the ball pad on the bottom surface of the laminate substrate as taught by Houghton et al. so that the bonding strength and the interconnect reliability can be improved in Sholley et al. and Ikata et al's structure.

Regarding claims 15 and 16, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 11 above, except each of the plurality of laminate substrate reference vias being electrically connected to the respective PCB reference via and the PCB via being connected to respective pad respectively.

Houghton et al. teach using a high frequency package comprising an antenna/heat sink element, the package including:

- a substrate comprising a dielectric material including a ceramic or a plastic/organic (Col. 2, line 22)
- connecting pads/terminals (40, 42, etc. in Fig. 1) comprising a variety of configurations such as pins, solder balls, etc. (Col. 5, line 10-25), and
- the package being connected to a PCB (10 in Fig. 1) having a plurality of reference/ground vias (40/28and 26 respectively in Fig. 1) where the pads/terminals of the package and the board (40/28 respectively in Fig. 1) are electrically connected to each of the respective reference/ground vias in the PCB to provide improved shielding around the device and the desired noise reduction (Col. 2, line 60- Col. 3, line 60)

(Fig. 1; Col. 4, line 65- Col. 5, line 10).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate each of the plurality of laminate substrate reference vias being electrically connected to the respective PCB reference via and the PCB via being connected to respective pad as taught by Houghton et al. so that the shielding effect can be improved and high frequency noise can be reduced in Sholley et al. and Ikata et al's structure.

Regarding claim 17, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 11 above, except the laminate substrate comprising an organic material.

Houghton et al. further teach the laminate substrate comprising an organic material (Col. 2, line 22).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the laminate substrate comprising an organic material as taught by Houghton et al. so that the mismatch in the thermal properties between the substrate and the PCB can be reduced and the processing can be simplified in Sholley et al. and Ikata et al's structure.

Regarding claim 20, Ikata et al. and Sholley et al. teach substantially the entire claimed structure as applied to claim 11 above, except each of the plurality of the laminate substrate reference vias being electrically connected to the respective ball pad on the bottom surface of the laminate substrate.

Houghton et al. teach using a high frequency package comprising an antenna/heat sink element, the package including:

- a substrate comprising a dielectric material including a ceramic or a plastic/organic (Col. 2, line 22)
- connecting pads/terminals (40, 42, etc. in Fig. 1) comprising a variety of configurations such as pins, solder balls, etc. (Col. 5, line 10-25), and

- the package being connected to a PCB (10 in Fig. 1) having a plurality of reference/ground vias (40/28and 26 respectively in Fig. 1) where the pads/terminals of the package and the board (40/28 respectively in Fig. 1) are electrically connected to each of the respective reference/ground vias in the PCB to provide improved shielding around the device and the desired noise reduction (Col. 2, line 60- Col. 3, line 60)

(Fig. 1; Col. 4, line 65- Col. 5, line 10).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate each of the plurality of the laminate substrate reference vias being electrically connected to the respective ball pad on the bottom surface of the laminate substrate as taught by Houghton et al. so that the bonding strength and the interconnect reliability can be improved in Sholley et al. and Ikata et al's structure.

Response to Arguments

4. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Nitin Parekh

NP
09-16-03